

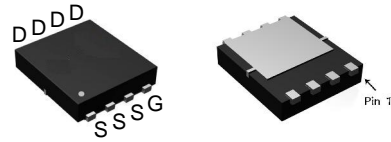
Features

- 30V/65A,
 $R_{DS(ON)} = 5.2m\Omega(\text{typ.}) @ V_{GS} = 10V$
 $R_{DS(ON)} = 6.7m\Omega(\text{typ.}) @ V_{GS} = 4.5V$
- Avalanche Rated
- 100% UIS + R_g Tested
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

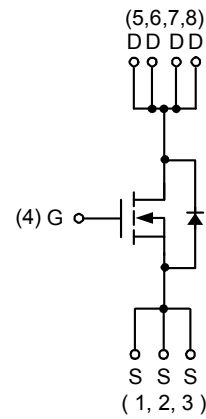
Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems.

Pin Description



DFN3.3x3.3_8L_EP1_P



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter		Rating	Unit
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	
I_D^d	Continuous Drain Current ($V_{GS}=10\text{V}$)	$T_C=25^\circ\text{C}$	65	A
		$T_C=70^\circ\text{C}$	49	
I_{DM}	Pulsed Drain Current ($V_{GS}=10\text{V}$)	$T_C=25^\circ\text{C}$	195	
I_S	Diode Continuous Forward Current		65	
I_{AS}^b	Avalanche Current, Single pulse	$L=0.1\text{mH}$	25	mJ
E_{AS}^b	Avalanche Energy, Single pulse	$L=0.1\text{mH}$	31.25	
T_J	Maximum Junction Temperature		150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		-55 to 150	
P_D^d	Maximum Power Dissipation	$T_C=25^\circ\text{C}$	29	W
		$T_C=70^\circ\text{C}$	19	
$R_{\theta JA}^{a,c}$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{s}$	35	$^\circ\text{C/W}$
		Steady State	60	
$R_{\theta JC}^d$	Thermal Resistance-Junction to Case	Steady State	3.5	

Note a : Surface Mounted on 1in^2 pad area, $t \leq 10\text{sec}$.

Note b : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_J=25^\circ\text{C}$).

Note c : Maximum under Steady State conditions is 75°C/W .

Note d : The power dissipation P_D is based on $T_{J(\text{MAX})} = 150^\circ\text{C}$, and it is useful for reducing junction-to-case thermal resistance ($R_{\theta JC}$) when additional heat sink is used.

Electrical Characteristics ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

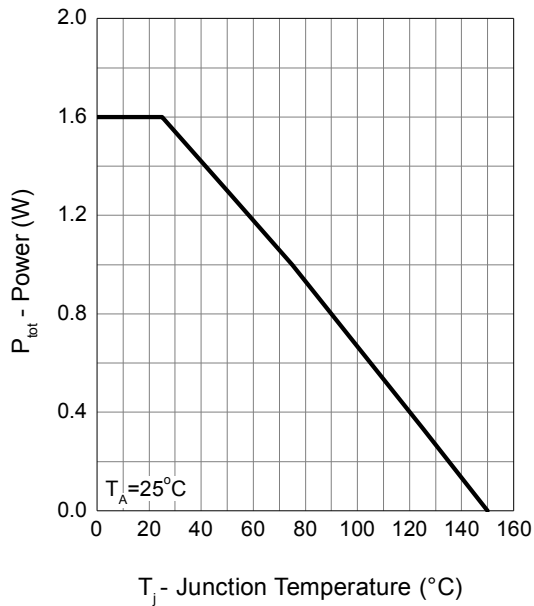
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$	-	-	1	μA
		$T_J=85^\circ\text{C}$	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.5	1.8	2.5	V
I_{GSS}	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
$R_{DS(ON)}^a$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=12A$	-	5.2	6	m Ω
		$V_{GS}=4.5V, I_{DS}=9A$	-	6.7	7.5	
Diode Characteristics						
V_{SD}^a	Diode Forward Voltage	$I_{SD}=2A, V_{GS}=0V$	-	0.8	1.1	V
t_{rr}^b	Reverse Recovery Time	$I_{SD}=12A, di_{SD}/dt=100A/\mu s$	-	10	-	ns
t_a	Charge Time		-	7	-	
t_b	Discharge Time		-	2.7	-	
Q_{rr}^b	Reverse Recovery Charge		-	3	-	
Dynamic Characteristics ^b						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1\text{MHz}$	-	3	4.5	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=15V,$ Frequency=1.0MHz	560	1100	1540	pF
C_{oss}	Output Capacitance		185	265	345	
C_{riss}	Reverse Transfer Capacitance		99	105	231	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=15V, R_L=15\Omega,$ $I_{DS}=1A, V_{GEN}=10V,$ $R_G=6\Omega$	-	14	26	ns
t_r	Turn-on Rise Time		-	10	19	
$t_{d(OFF)}$	Turn-off Delay Time		-	44	80	
t_f	Turn-off Fall Time		-	12	23	
Gate Charge Characteristics ^b						
Q_g	Total Gate Charge	$V_{DS}=15V, V_{GS}=10V,$ $I_{DS}=12A$	-	28.3	39.6	nC
Q_g	Total Gate Charge	$V_{DS}=15V, V_{GS}=4.5V,$ $I_{DS}=12A$	-	12.9	18	
Q_{gth}	Threshold Gate Charge		-	2.46	3.44	
Q_{gs}	Gate-Source Charge		-	4.22	5.9	
Q_{gd}	Gate-Drain Charge		-	7.3	10.2	

 Note a : Pulse test ; pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.

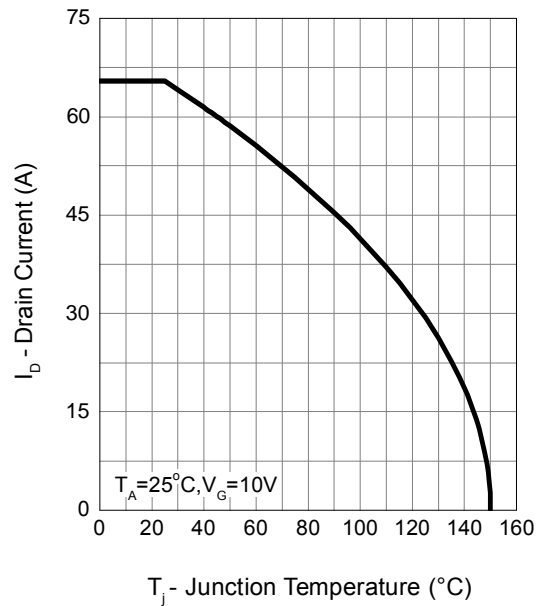
Note b : Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

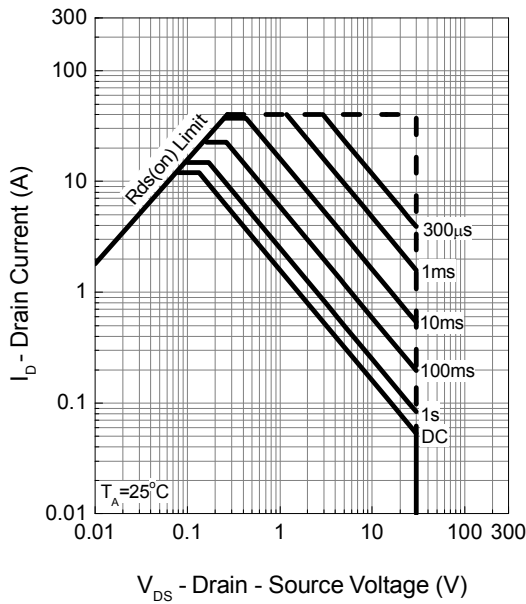
Power Dissipation



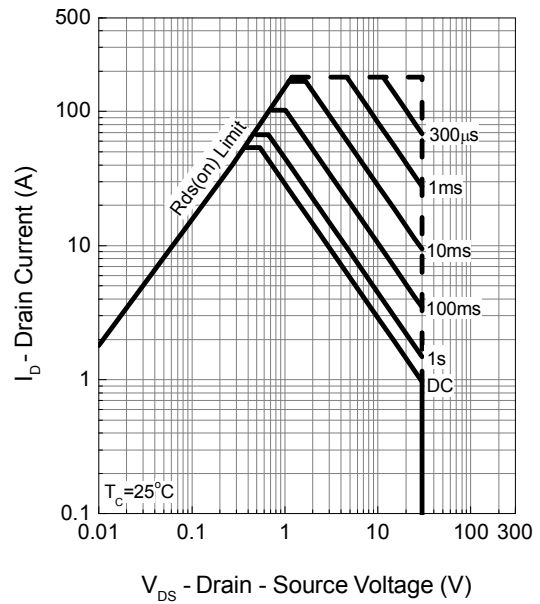
Drain Current



Safe Operation Area

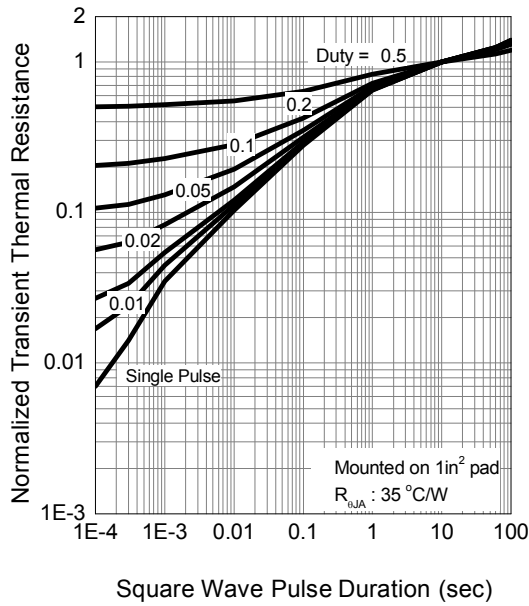


Safe Operation Area

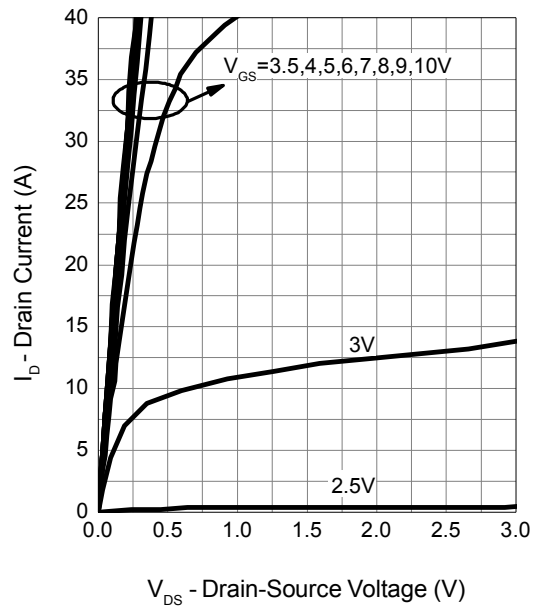


Typical Operating Characteristics (Cont.)

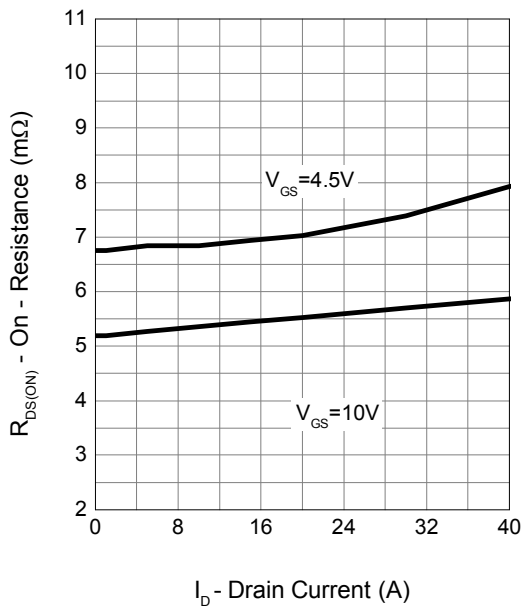
Thermal Transient Impedance



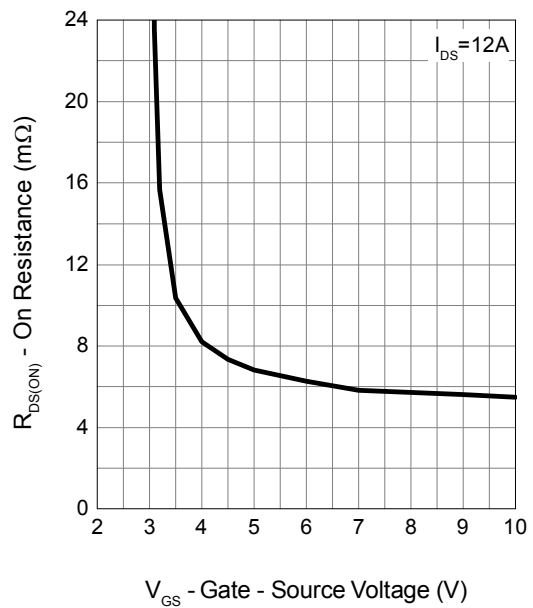
Output Characteristics



Drain-Source On Resistance

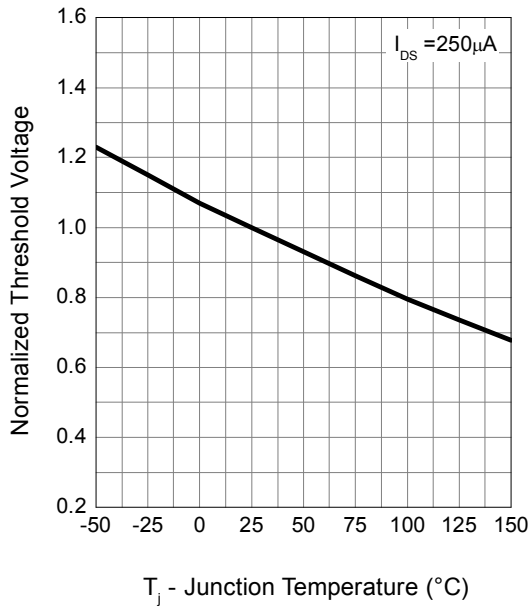


Gate-Source On Resistance

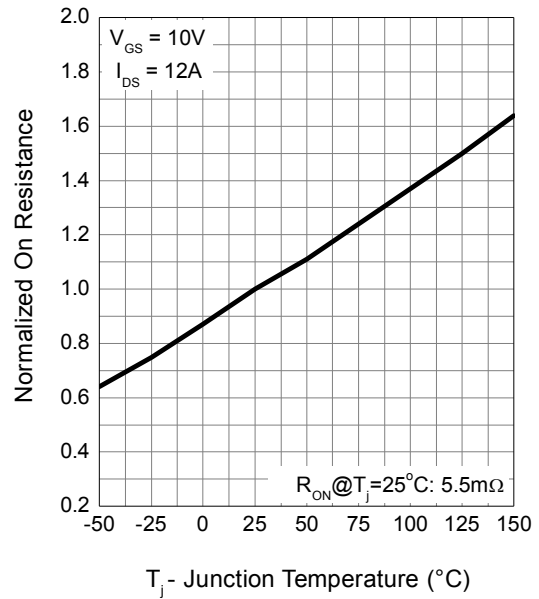


Typical Operating Characteristics (Cont.)

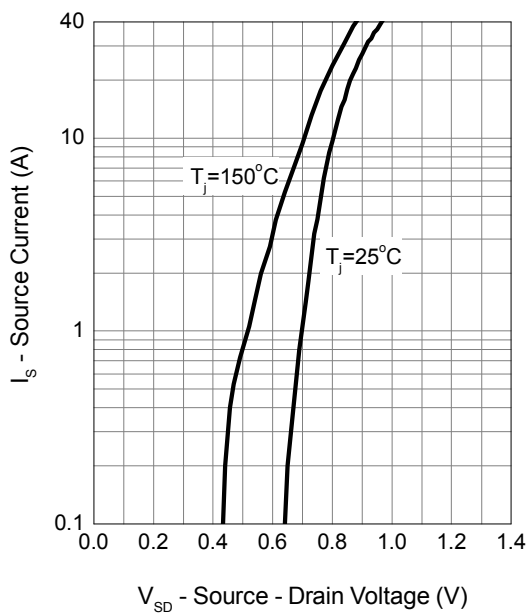
Gate Threshold Voltage



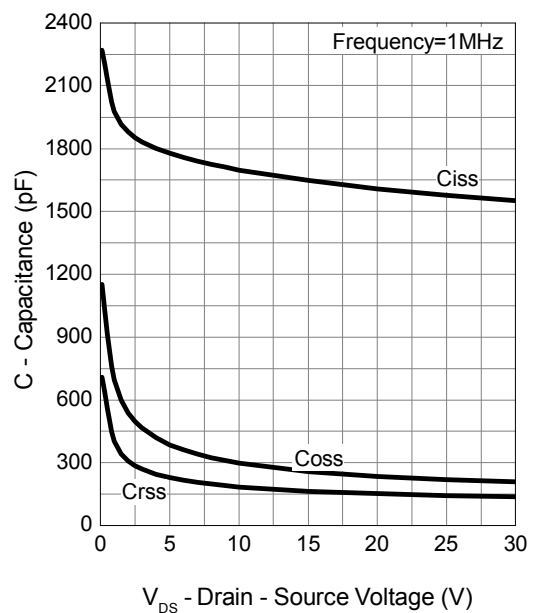
Drain-Source On Resistance



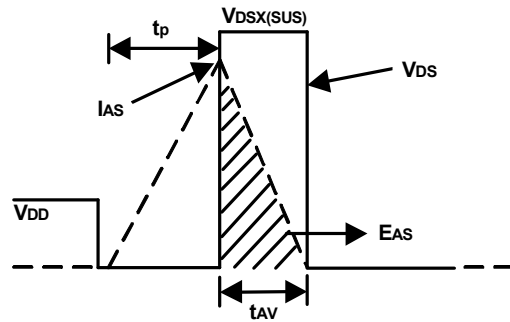
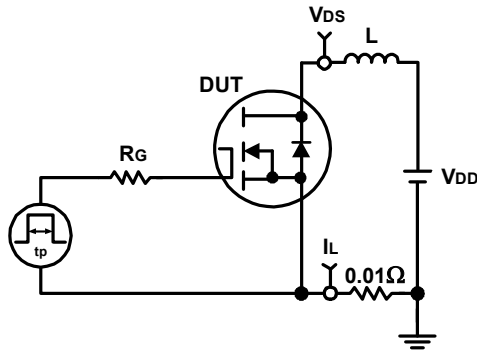
Source-Drain Diode Forward



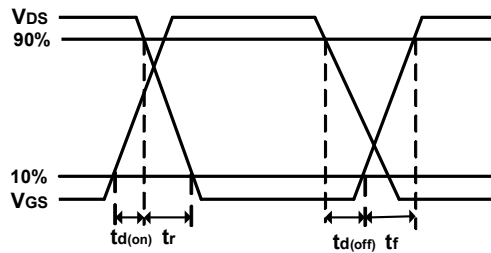
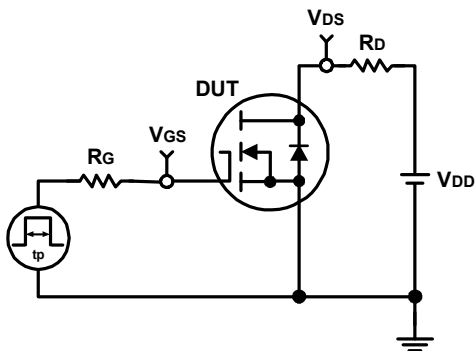
Capacitance



Avalanche Test Circuit and Waveforms

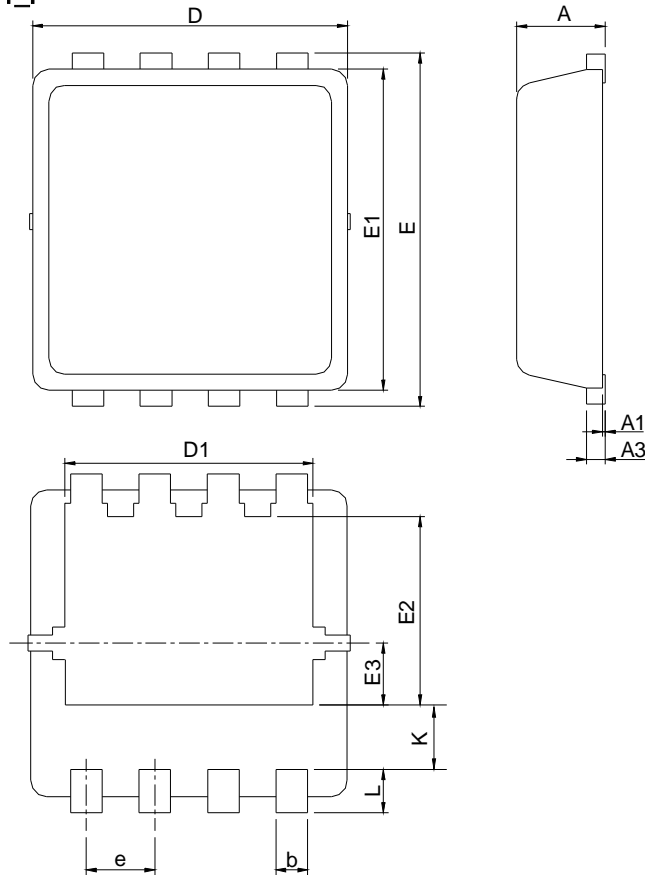


Switching Time Test Circuit and Waveforms



Package Information

DFN3.3x3.3_8L_EP1_P



SYMBOL	DFN3x3-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.10	0.25	0.004	0.010
b	0.24	0.35	0.009	0.014
D	2.90	3.10	0.114	0.122
D1	2.25	2.45	0.089	0.096
E	3.10	3.30	0.122	0.130
E1	2.90	3.10	0.114	0.122
E2	1.65	1.85	0.065	0.073
E3	0.56	0.58	0.022	0.023
e	0.65 BSC		0.026 BSC	
K	0.475	0.775	0.019	0.031
L	0.30	0.50	0.012	0.020

RECOMMENDED LAND PATTERN

