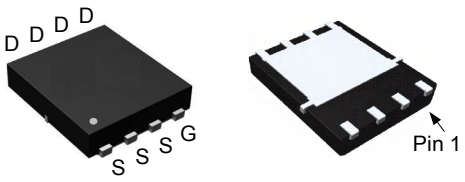
- 40V/150A
- $R_{DS(ON)}$=2mΩ (typ) @VGS=10V
  $R_{DS(ON)}$=3mΩ (typ) @VGS=4.5V
- 100% UIS & RG Tested
- Reliableand Rugged
- Lead Freeand Green Devices Available
  (RoHS Compliant)

## Applications

- Power Management for Industrial DC/DC Converters

## Pin Description

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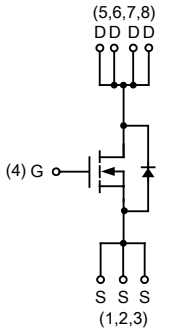



N-Channel MOSFET

## Absolute Maximum Ratings ($T_A$= 25°C unless otherwise noted)

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| **Common Ratings** | | | | |
| $V_{DSS}$ | Drain-Source Voltage | | 40 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | |
| $I_D$ [G] | Continuous Drain Current | Tc=25°C | 150 | A |
| | | Tc=25°C | 150 | |
| | | Tc=100°C | 113 | |
| $I_{DM}$ [C] | Pulsed Drain Current | | 450 | |
| $P_D$ [B] | Power Dissipation | $T_C$=25°C | 120 | W |
| | | $T_C$=100°C | 80 | |
| $I_S$ [G] | Diode Continuous Forward Current | | 150 | A |
| $T_{STG}$, $T_j$ | Storage Temperature Range | | -55 to 150 | °C |
| $I_{AS}$ [C] | Single pulsed avalanlce Current | | 47 | A |
| $E_{AS}$ [C] | Single pulsed avalanlce energy | L=0.3mH | 331 | mJ |
| $R_{\theta JC}$ | Thermal Resistance-Junction to Case | | 0.8 | °C/W |
| $R_{\theta JA}$ [AD] | Thermal Resistance-Junction to Ambient | t≤10S | 20 | |
| | | Steady State | 50 | |

**Electrical Characteristics ($T_J$=25°C unless otherwise noted)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=250µA, $V_{GS}$=0V | 40 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=40V, $V_{GS}$=0V | | | 1 | µA |
| | | $T_J$=55°C | | | 5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±20V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250µA | 1 | 1.9 | 2.5 | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=20A | | 2 | 3.5 | mΩ |
| | | $T_J$=125°C | | 3.25 | 4 | |
| | | $V_{GS}$=4.5V, $I_D$=20A | | 3 | 4.5 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=5V, $I_D$=20A | | 100 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1A, $V_{GS}$=0V | | 0.7 | 1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current [G] | | | | 120 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=20V, f=1MHz | | 5225 | | pF |
| $C_{oss}$ | Output Capacitance | | | 895 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 200 | | pF |
| $R_g$ | Gate resistance | f=1MHz | 1 | 2 | 3.1 | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$(10V) | Total Gate Charge | $V_{GS}$=10V, $V_{DS}$=20V, $I_D$=20A | | 68 | 95 | nC |
| $Q_g$(4.5V) | Total Gate Charge | | | 28 | 40 | nC |
| $Q_{gs}$ | Gate Source Charge | | | 16.5 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 4.5 | | nC |
| $Q_{oss}$ | Output Charge | $V_{GS}$=0V, $V_{DS}$=20V | | 37 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=10V, $V_{DS}$=20V, $R_L$=1Ω, $R_{GEN}$=3Ω | | 12.5 | | ns |
| $t_r$ | Turn-On Rise Time | | | 9.5 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 57.5 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 10.5 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=20A, di/dt=500A/µs | | 20 | | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=20A, di/dt=500A/µs | | 60 | | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25° C.
I. The maximum current rating is silicon limited

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

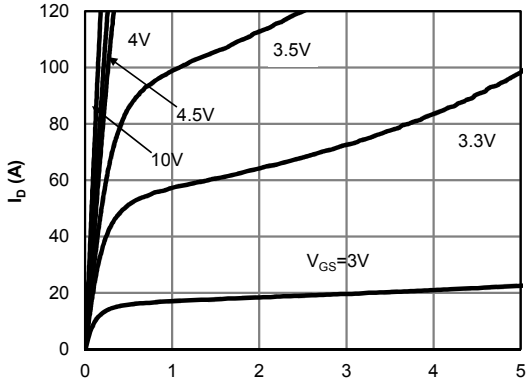



**Figure 1: On-Region Characteristics (Note E)**

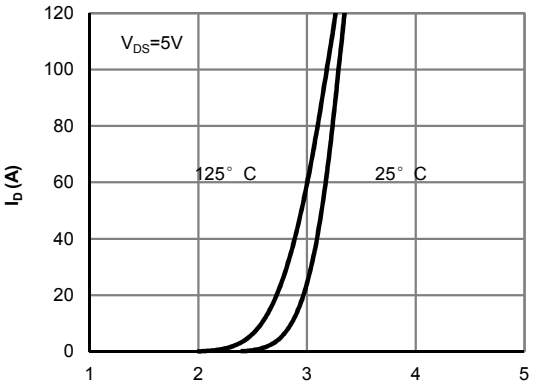



**Figure 2: Transfer Characteristics (Note E)**

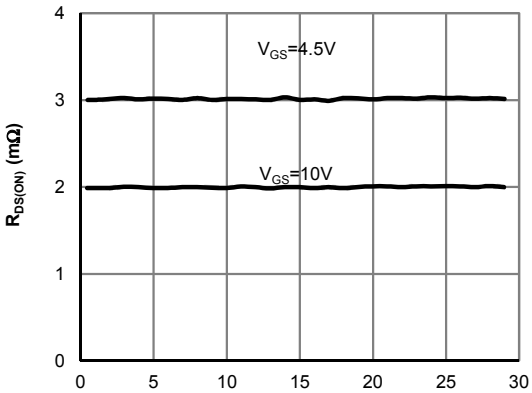



**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**

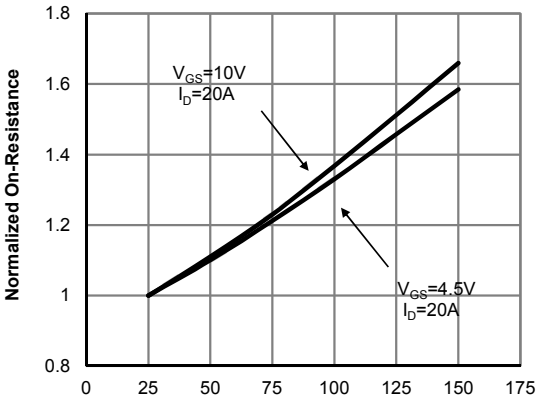



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

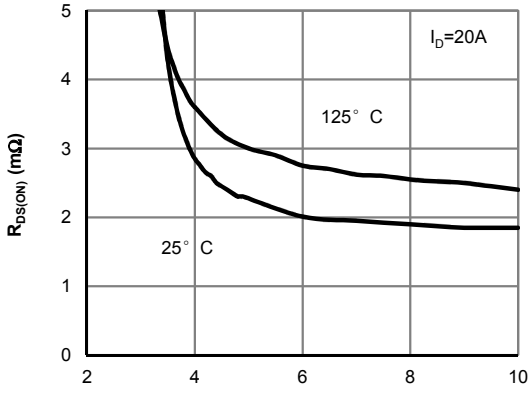



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

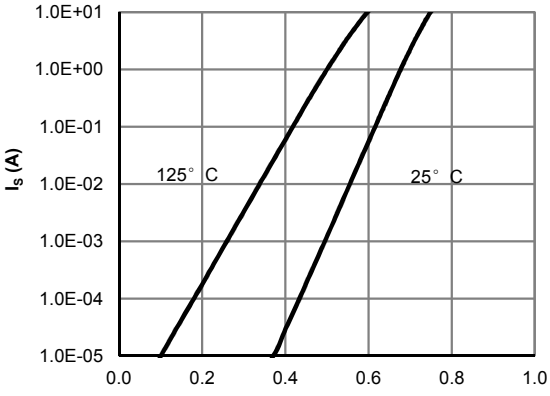



**Figure 6: Body-Diode Characteristics (Note E)**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

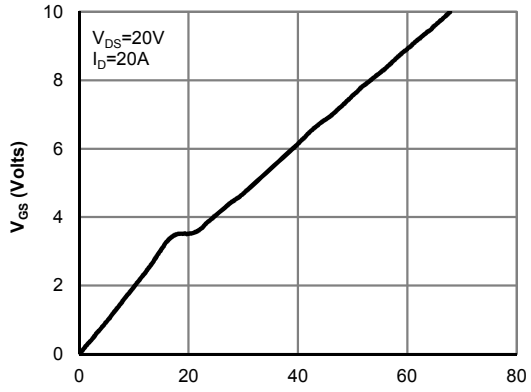



**Figure 7: Gate-Charge Characteristics**

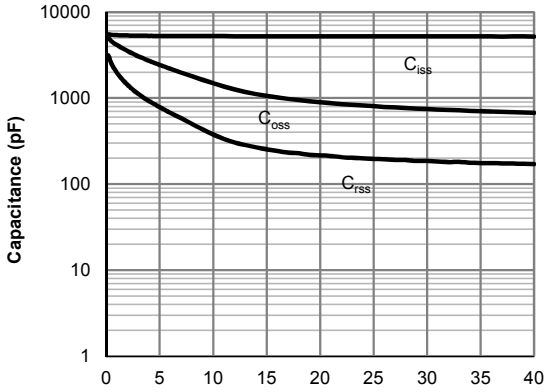



**Figure 8: Capacitance Characteristics**

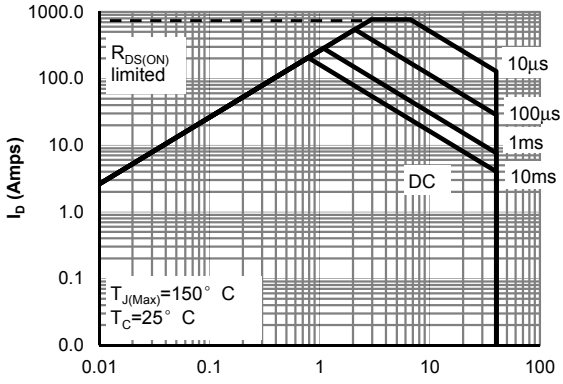



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

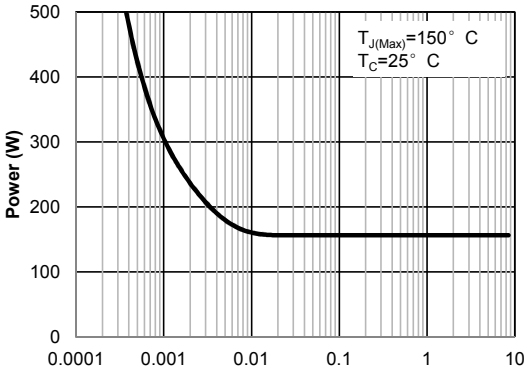



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

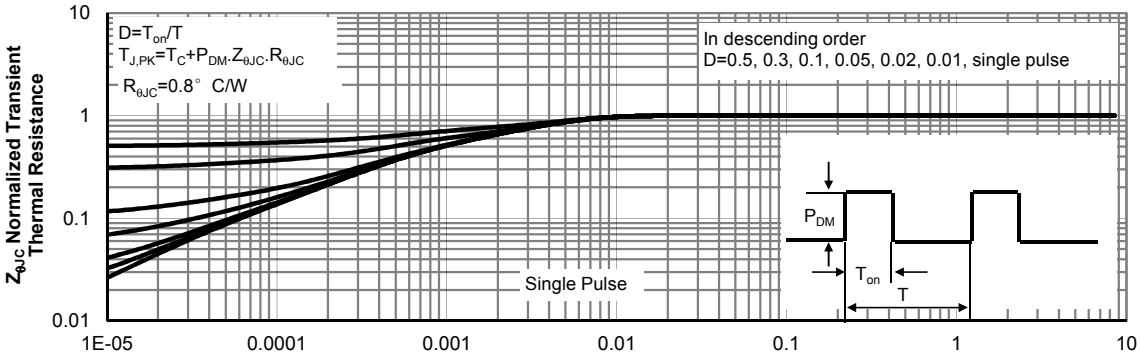



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

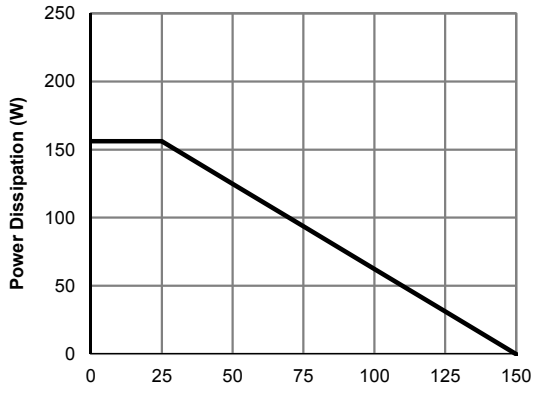



**Figure 12: Power De-rating (Note F)**

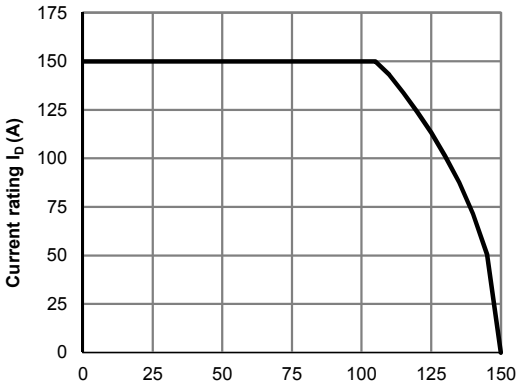



**Figure 13: Current De-rating (Note F)**

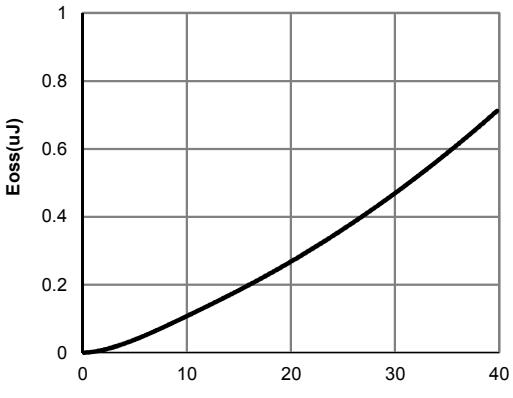



**Figure 14: Coss stored Energy**

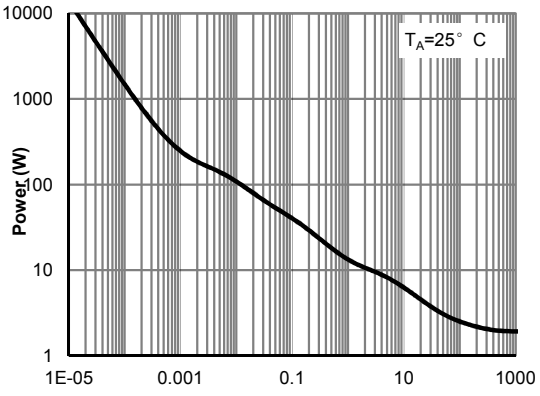



**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

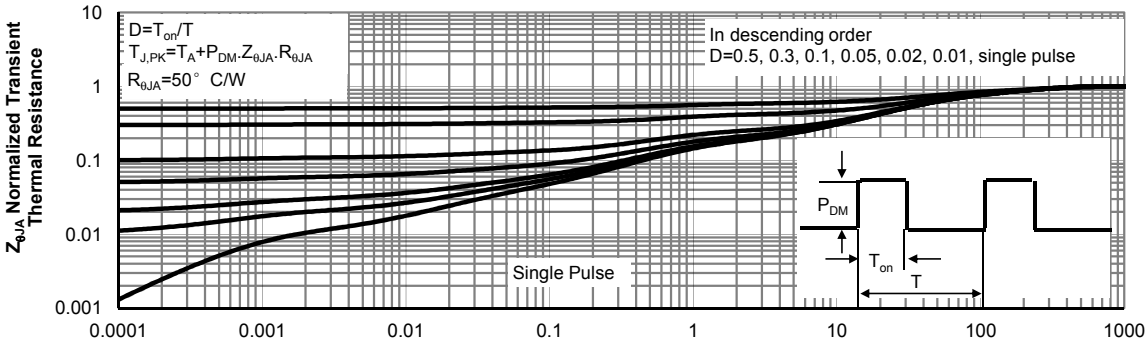



**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

Figure A: Gate Charge Test Circuit & Waveforms

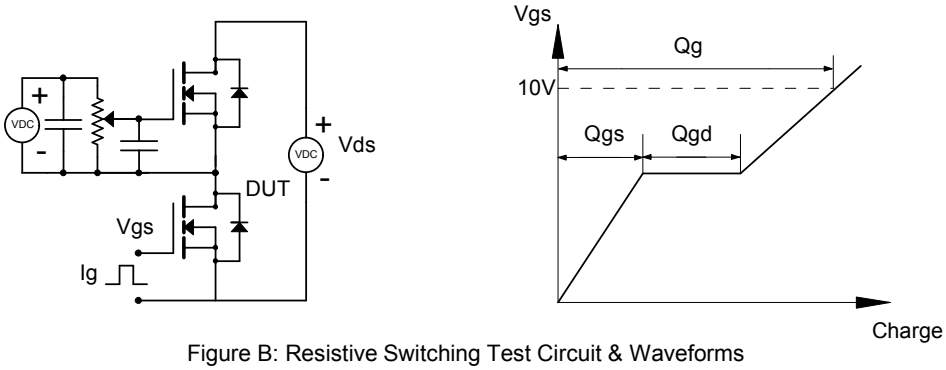



Figure B: Resistive Switching Test Circuit & Waveforms

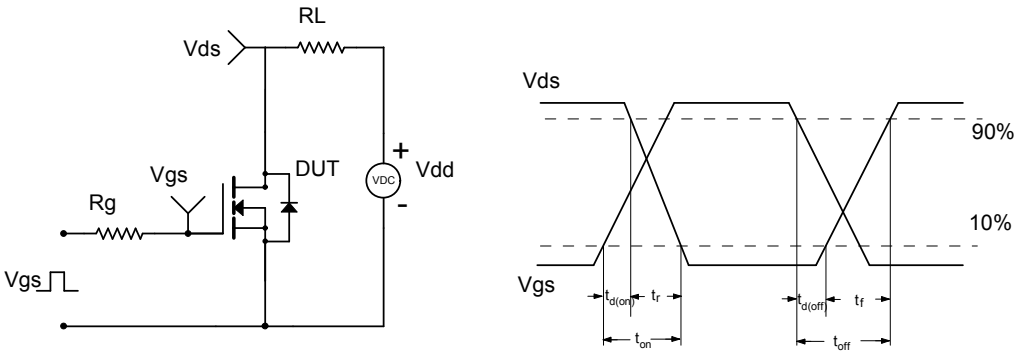



Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

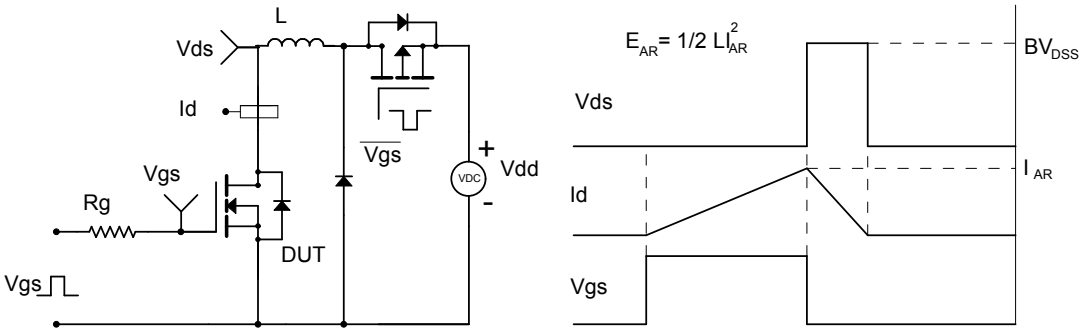
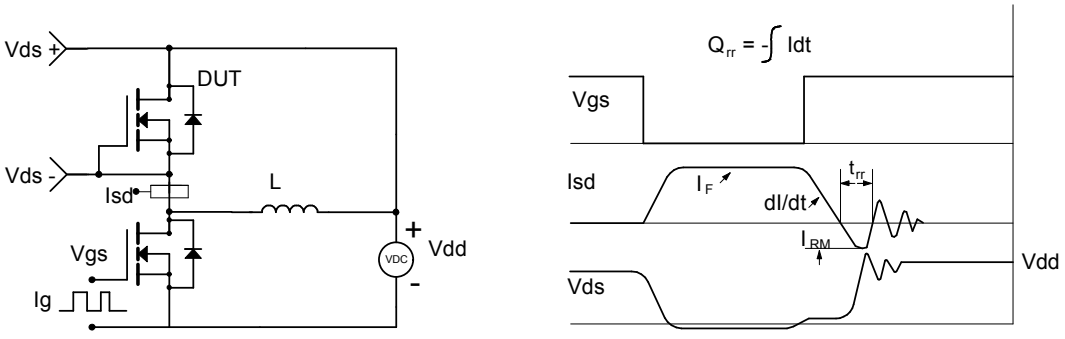



Figure D: Diode Recovery Test Circuit & Waveforms



# PDFN5*6 OUTLINE