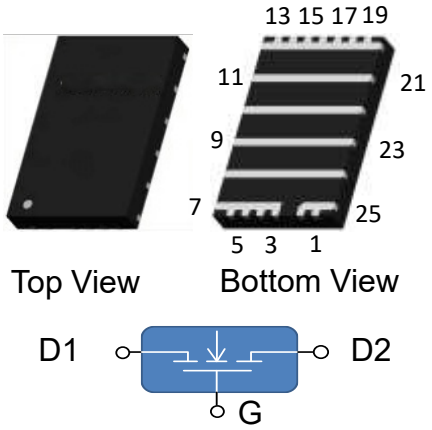
Features

- Bi-directional blocking capability
- GaN-on-Silicon E-mode HEMT technology
- Ultra-low on resistance



Applications

- BMS battery protection
- High side load switch in bi-directional converter
- Switch circuits in multiple power supplier system

Package Marking and Ordering Information

Device	Marking	Package	Qty
RSTGE030E10VFQ	GE030E10VFQ	FCQFN4x6	2500pcs

Key Performance Parameters

Key performance parameters at T_J = 25 °C

Parameter	Value	Unit
$V_{DD,\ max}$	100	V
$R_{DD(on),typ}$ @ V_G = 5 V	2.3	mΩ
$R_{DD(on),max}$ @ V_G = 5 V	3	mΩ
$Q_{G,typ}$ @ V_{DD} = 50 V	70	nC
$I_{D,Pulse}$ (T_J = 25 ˚C)	370	A
Q_{OSS} @ V_{DD} = 50 V	65	nC

Pin Information

Pin	Pin Description	Pin Function
1,2,25	Gate	Driver Gate
3,7,9,11,21,23	Drain1	Power Drain1
8,10,12-20,22,24	Drain2	Power Drain2

Maximum Ratings

at T_J = 25 °C unless otherwise specified.
Exceeding the maximum ratings may destroy the device.

SYMBOL	PARAMETER	MAX	UNIT
V_{DD}	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	100	V
$V_{DD(tr)}$	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage [1] (V_{GD} = 0 V, 1h total time, $T_A = T_{JMAX}$)	120	V
I_D	Continuous Current (V_{GD} = 5 V, T_B = 25 ˚C，$R_{\theta JB}$ = 1.9 ˚C/W)	101	A
	Continuous Current (V_{GD} = 5 V, T_B = 100 ˚C，$R_{\theta JB}$ = 1.9 ˚C/W)	64	A
	Continuous Current (V_{GD} = 5 V, T_A = 25 ˚C，$R_{\theta JA}$ = 38.4 ˚C/W)	22	A
	Pulsed (V_{GD} = 5 V, T_J = 25 ˚C, T_{Pulse} = 100 μs)	370	A
	Pulsed (V_{GD} = 5 V, T_J = 150 ˚C, T_{Pulse} = 100 μs)	280	A
V_{DG}	Drain1-to-Gate Voltage or Drain2-to-Gate Voltage	100	V
V_{GD}	Gate-to-Drain1 Voltage or Gate-to-Drain2 Voltage	6	V
P_{tot}	Power Dissipation (V_{GD} = 5 V, T_B =25˚C，$R_{\theta JB}$ = 1.9 ˚C/W)	65	W
	Power Dissipation (V_{GD} = 5 V, T_A =25˚C，$R_{\theta JA}$ = 38.4 ˚C/W)	3.3	W
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

Note:
1，Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation;

Thermal Characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	16.74	˚C/W	-
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.91	˚C/W	-
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [2]	38.38	˚C/W	-
T_{sold}	Maximum Reflow Soldering Temperature	260	°C	MSL3

Note:
2, RθJA is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is mounted in horizontal position without air stream cooling.

Electric Characteristics

at TJ = 25 °C, unless otherwise specified.
Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{D1D2}	Drain1-to-Drain2 Leakage	-	1	4	μA	$V_{D2} = V_G = 0$ V, $V_{D1} = 80$ V
	Drain1-to-Drain2 Leakage ($T_J = 125$ ˚C)	-	200	-	μA	$V_{D2} = V_G = 0$ V, $V_{D1} = 80$ V
I_{D2D1}	Drain2-to-Drain1 Leakage	-	1	4	μA	$V_{D1} = V_G = 0$ V, $V_{D2} = 80$ V
	Drain2-to-Drain1 Leakage ($T_J = 125$ ˚C)	-	200	-	μA	$V_{D1} = V_G = 0$ V, $V_{D2} = 80$ V
I_{GD}	Gate-to-Drain Forward Leakage	-	0.5	4	μA	$V_{D1} = V_{D2} = 0$ V, $V_G = 5$ V
	Gate-to-Drain Forward Leakage ($T_J = 125$ ˚C)	-	70	-	μA	$V_{D1} = V_{D2} = 0$ V, $V_G = 5$ V
	Gate-to-Drain Forward Leakage	-	1	8	μA	$V_{D1} = V_{D2} = 0$ V, $V_G = 5.5$ V
	Gate-to-Drain Forward Leakage ($T_J = 125$ ˚C)	-	140	-	μA	$V_{D1} = V_{D2} = 0$ V, $V_G = 5.5$ V
	Gate-to-Drain Forward Leakage	-	2	18	μA	$V_{D1} = V_{D2} = 0$ V, $V_G = 6$ V
	Gate-to-Drain Forward Leakage ($T_J = 125$ ˚C)	-	280	-	μA	$V_{D1} = V_{D2} = 0$ V, $V_G = 6$ V
$V_{GD1(TH)}$	Gate Threshold Voltage [3]	0.8	1.3	2.5	V	$V_{D1} = 0$ V, $V_{D2} = V_G$, $I_{D2D1} = 11.5$ mA
$V_{GD2(TH)}$	Gate Threshold Voltage [3]	0.8	1.3	2.5	V	$V_{D2} = 0$ V, $V_{D1} = V_G$, $I_{D1D2} = 11.5$ mA
$R_{D1D2(on)}$	Drain1-to-Drain2 On-state Resistance [3]	-	2.3	3	mΩ	$V_{D2} = 0$ V, $V_{GD} = 5$ V, $I_{D1D2} = 2$ A
$R_{D2D1(on)}$	Drain2-to-Drain1 On-state Resistance [3]	-	2.3	3	mΩ	$V_{D1} = 0$ V, $V_{GD} = 5$ V, $I_{D2D1} = 2$ A
V_{D1D2}	Drain1-to-Drain2 Forward Voltage	-	1.9	-	V	$I_{D1} = 25$ A, $V_G = 0$ V
V_{D2D1}	Drain2-to-Drain1 Forward Voltage	-	1.9	-	V	$I_{D2} = 25$ A, $V_G = 0$ V

Note:
3, VGD1(TH), VGD2(TH), RD1D2(on) and RD2D1(on) are measured without prior drain bias or switching stress.

Dynamic characteristics [4]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	2820	-	pF	V_G = 0 V, V_D = 50 V
C_{OSS}	Output Capacitance	-	680	-		V_G = 0 V, V_D = 50 V
C_{RSS}	Reverse Transfer Capacitance	-	380	-		V_G = 0 V, V_D = 50 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	950	-		V_G = 0 V, V_D = 0 V to 50 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	1300	-		V_G = 0 V, V_D = 0 V to 50 V
R_G	Gate Resistance	-	5	-	Ω	f =5 MHz, open drain
Q_G	Total Gate Charge	-	70	-	nC	V_D = 50 V, V_G = 5 V, I_D = 25 A
Q_{GD1}	Gate-to-Drain1 Charge (V_{D2D1}=50V)	-	5.2	-		V_{D1} = 0 V, V_{D2} = 50 V, I_{D2D1} = 25 A
Q_{GD1}	Gate-to-Drain1 Charge (V_{D1D2}=50V)	-	48	-		V_{D2} = 0 V, V_{D1} = 50 V, I_{D1D2} = 25 A
Q_{GD2}	Gate-to-Drain2 Charge (V_{D1D2}=50V)	-	5.2	-		V_{D2} = 0 V, V_{D1} = 50 V, I_{D1D2} = 25 A
Q_{GD2}	Gate-to-Drain2 Charge (V_{D2D1}=50V)	-	48	-		V_{D1} = 0 V, V_{D2} = 50 V, I_{D2D1} = 25 A
V_{Plat}	Gate Plateau Voltage	-	1.8	-	V	I_D = 25 A, V_D = 50 V, V_G = 0 V to 5 V
$Q_{G(TH)}$	Gate Charge at Threshold	-	3.2	-	nC	V_G = 5 V, V_D = 0 V to 50 V, I_D = 25 A
Q_{OSS}	Output Charge	-	65	-		V_G = 0 V, V_D = 0 V to 50 V
Q_{RR}	Reverse Recovery Charge	-	0	-		V_{DD} = 50 V, I_D = 25 A

Note:
Guaranteed by design.

Electric Characteristics Diagrams at T_J = 25 °C, unless specified otherwise

Fig. 1 Typ. Output Characteristics (TJ = 25 ˚C)

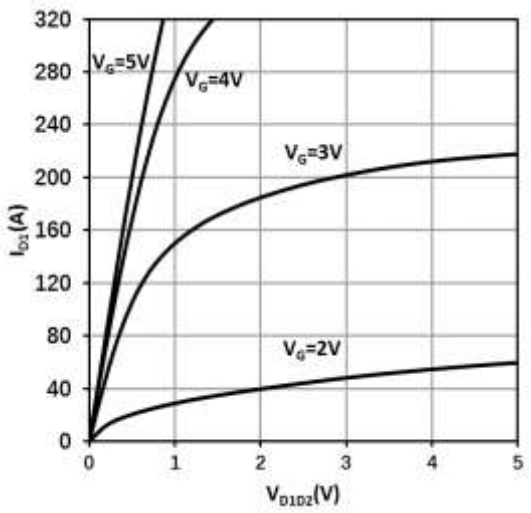


Fig. 2 Typ. Output Characteristics (TJ = 125 ˚C)

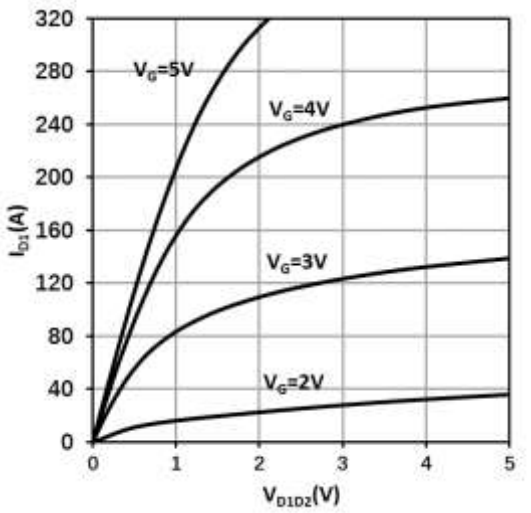


Fig. 3 Typ. Drain On-state Resistance (TJ = 25 ˚C)

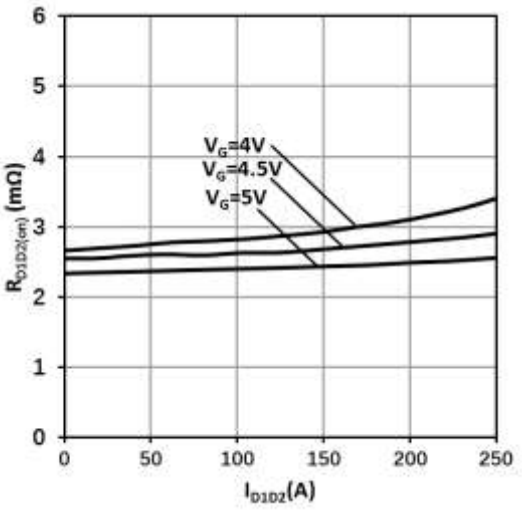
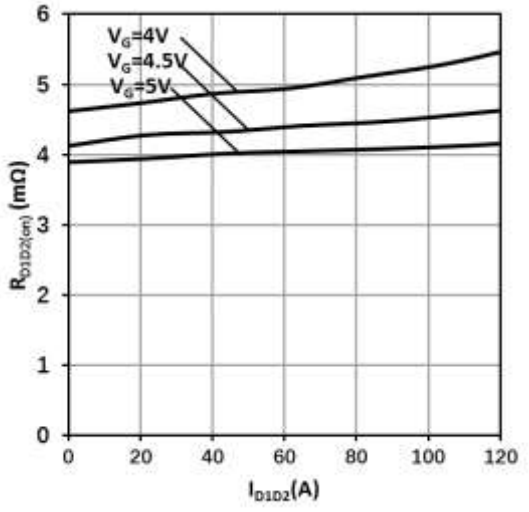


Fig. 4 Typ. Drain On-state Resistance (TJ = 125 ˚C)



Electric Characteristics Diagrams at T_J = 25 °C, unless specified otherwise

Fig. 5 Normalized On-State Resistance vs. Temp.

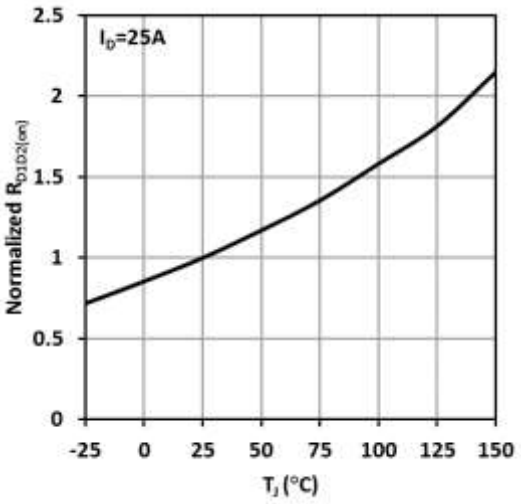


Fig. 6 Typ. Transfer Characteristics

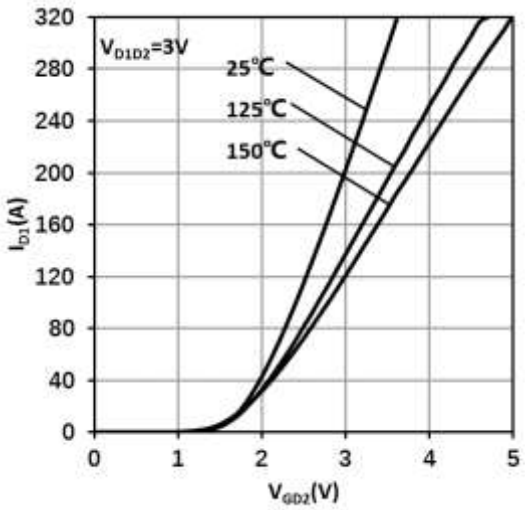


Fig. 7 Typ. Reverse Drain1- Drain2 Characteristics (VGD2 ≤ 0,TJ = 25 ˚C)

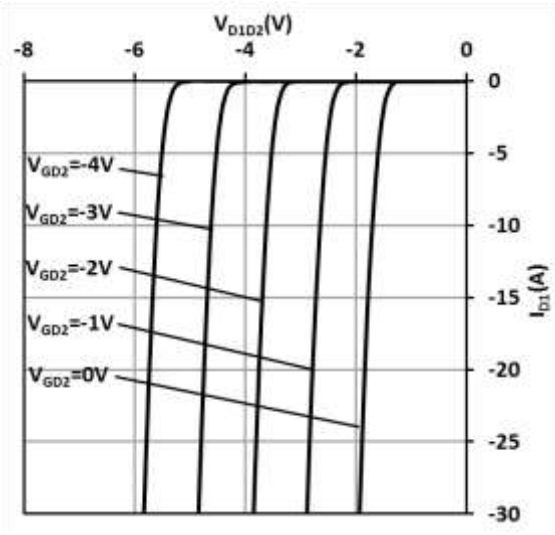
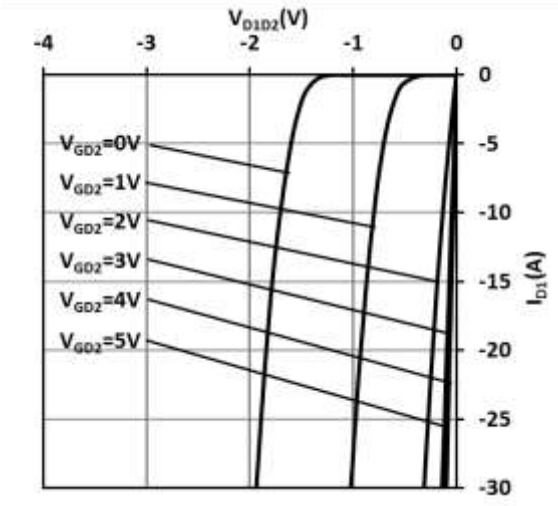


Fig. 8 Typ. Reverse Drain1- Drain2 Characteristics (VGD2 ≥ 0,TJ = 25 ˚C)



Electric Characteristics Diagrams at T_J = 25 °C, unless specified otherwise

Fig. 9 Typ. Reverse Drain1- Drain2 Characteristics (VGD2 ≤ 0,TJ = 125 ˚C)

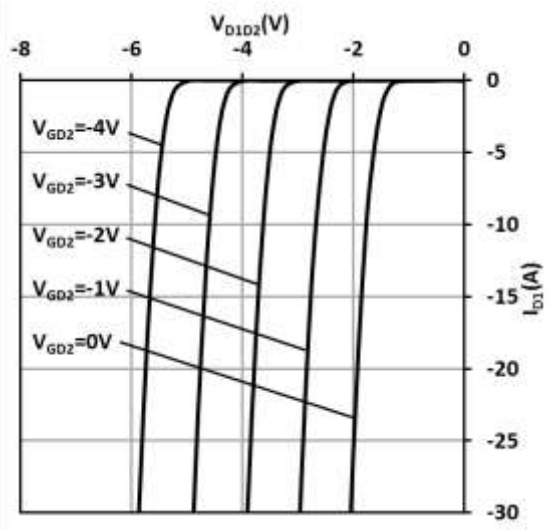


Fig. 10 Typ. Reverse Drain1- Drain2 Characteristics (VGD2 ≥ 0,TJ = 125 ˚C)

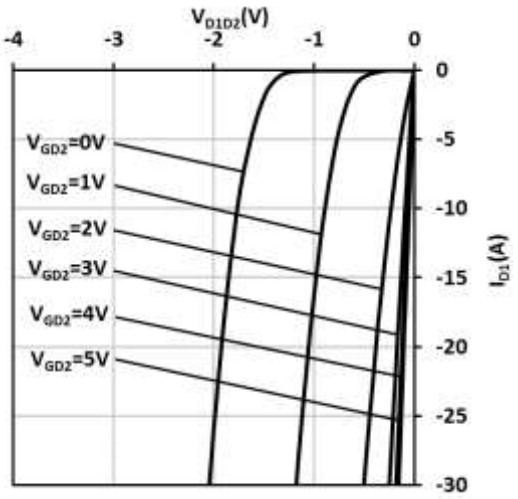


Fig. 11 Typ. Capacitances Characteristics

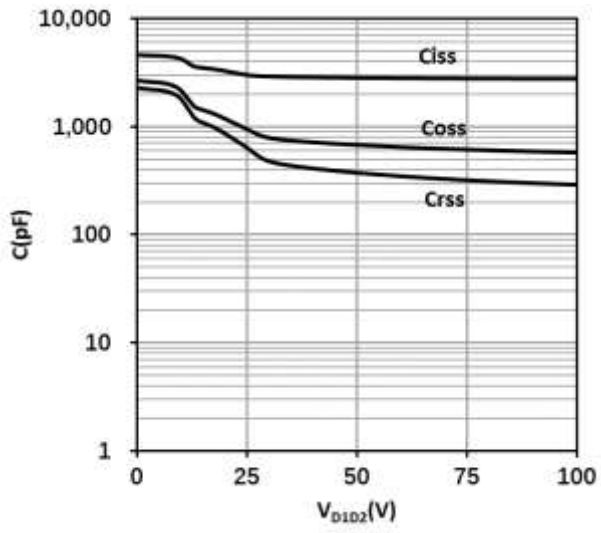
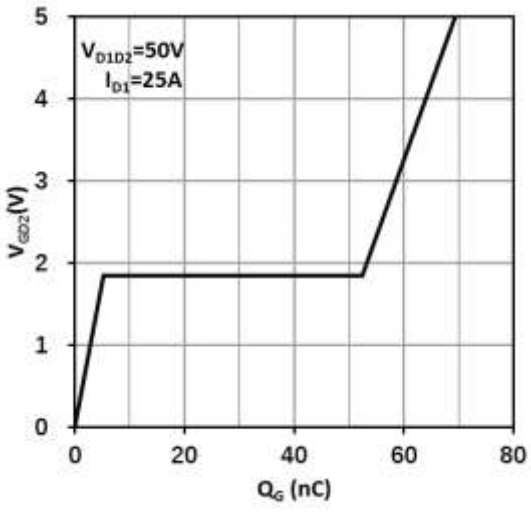


Fig. 12 Typ. Gate Charge



Electric Characteristics Diagrams at T_J = 25 °C, unless specified otherwise

Fig. 13 Normalized Threshold Voltage vs. Temp.

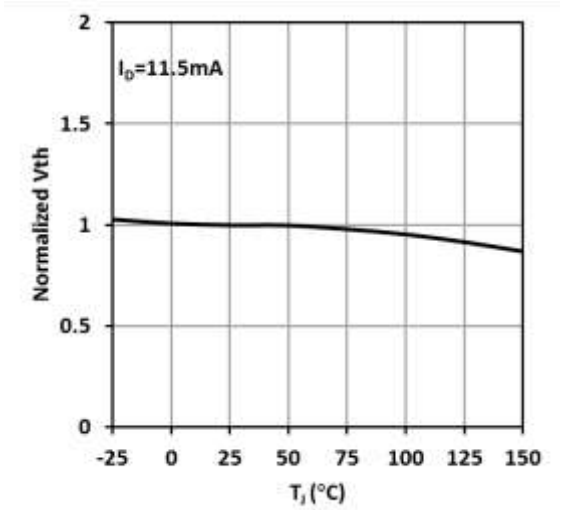


Fig. 14 Typ. Output Charge

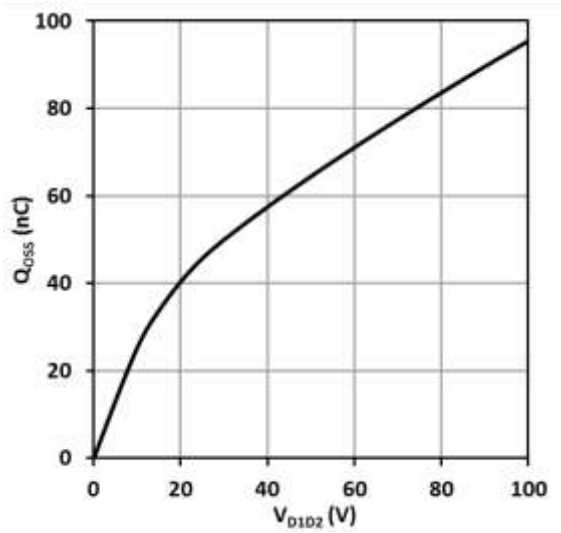


Fig. 15 Typ. Output Capacitance Stored Energy

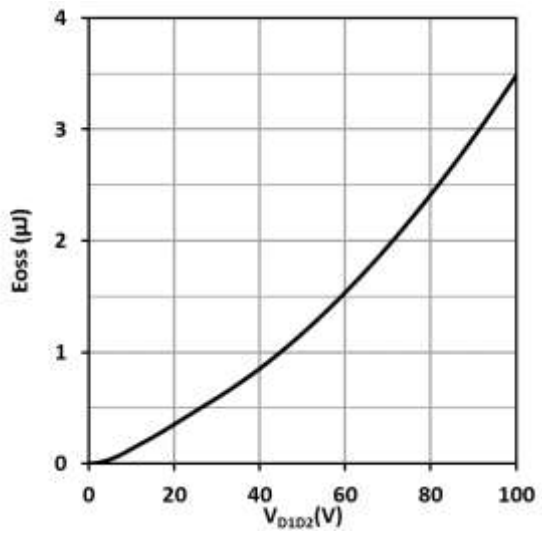
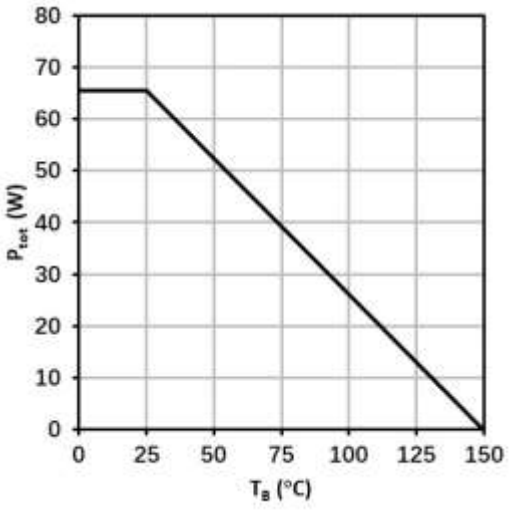


Fig. 16 Power Dissipation Ptot = f(TC), RθJB = 1.9˚C/W



Electric Characteristics Diagrams at T_J = 25 °C, unless specified otherwise

Fig. 17 Power Dissipation Ptot = f(TA), RθJA =38.4˚C/W

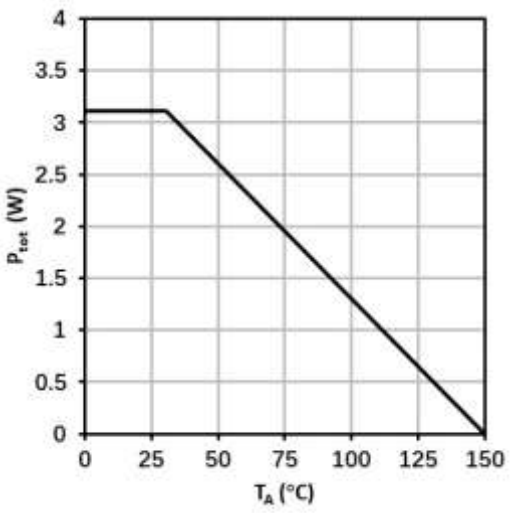


Fig. 18 Typ. Gate-to-Drain1 Leakage Characteristics
IG = f(VGD1); Drain2 Open

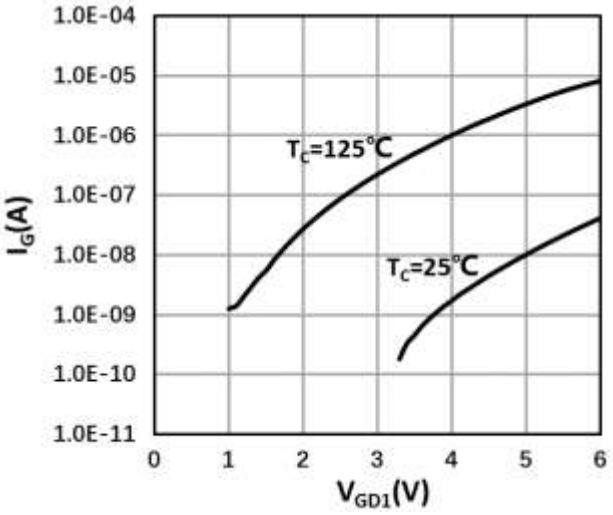


Fig. 19 Typ. Drain-source Leakage Characteristics
ID1D2 = f(VD1D2); VGD2 = 0 V

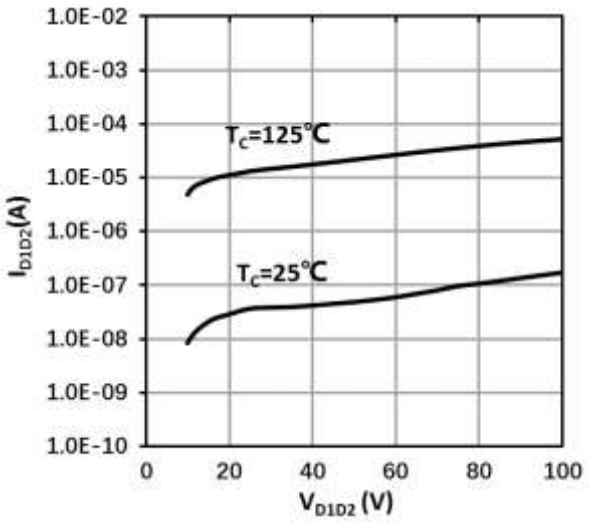
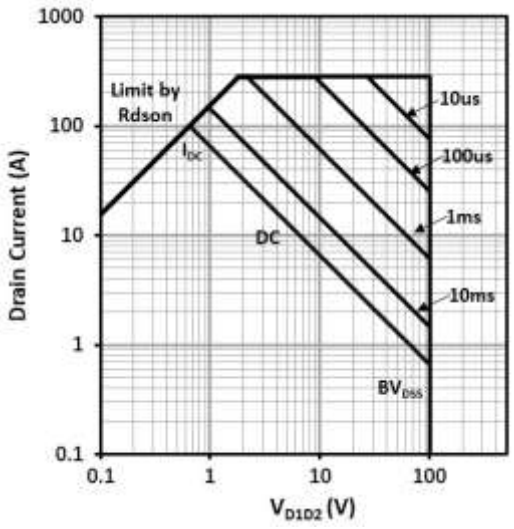
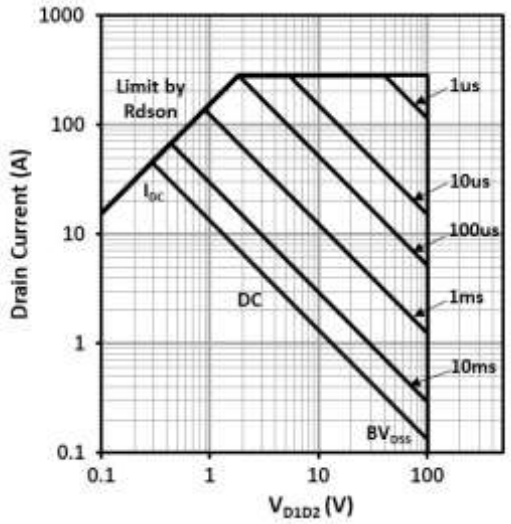
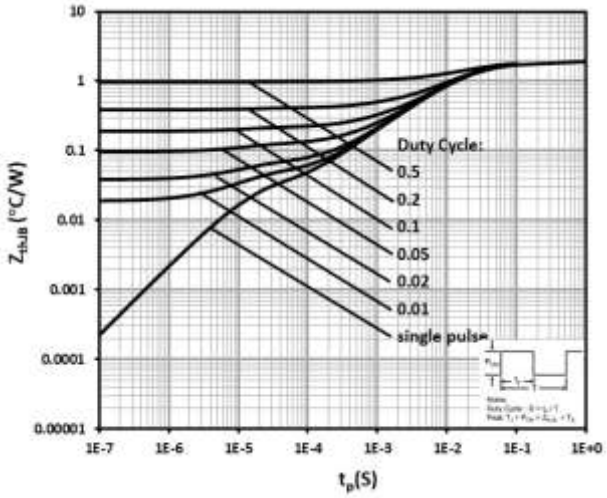


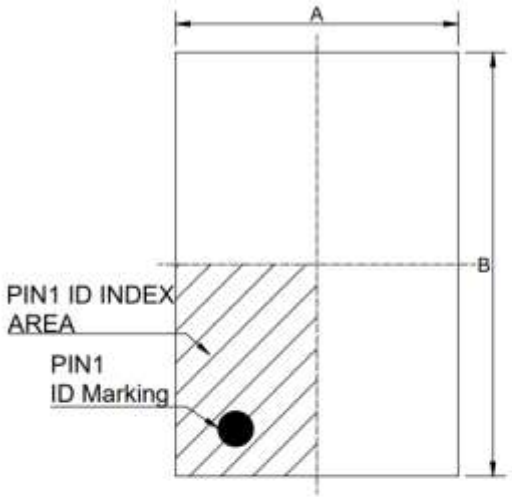
Fig. 20 Safe Operating Area
ID = f(VD1D2); TB = 25 ˚C; Single Pulse; Parameter: tp



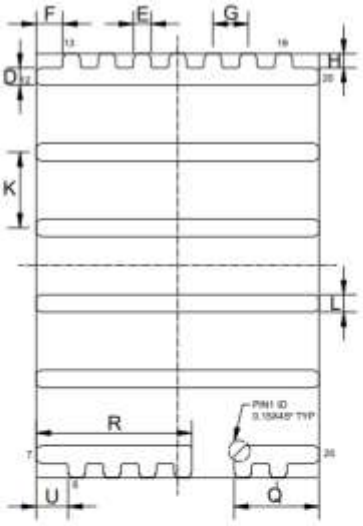
Electric Characteristics Diagrams at T_J = 25 °C, unless specified otherwise

Fig. 21 Safe Operating Area ID = f(VD1D2); TB = 125 ˚C; Single Pulse; Parameter: tp	Fig. 22 Max. Transient Thermal Impedance ZthJB = f(tp); Parameter: D=tp/T
	

Package Outlines

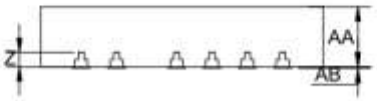


TOP VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.9	4.0	4.1	
B	5.9	6.0	6.1	
D	0.20	0.25	0.30	3X
E	0.20	0.25	0.30	13X
F		0.375 REF		2X
G		0.5 BASIC		10X
H		0.2 REF		3X
K		1.07 BASIC		6X
L	0.20	0.25	0.30	4X
Q	1.1	1.2	1.3	
R	2.1	2.2	2.3	
U		0.45 REF		2X
Z		0.203 REF		
AA	0.75	0.85	0.95	
AB	0.00	0.02	0.05	

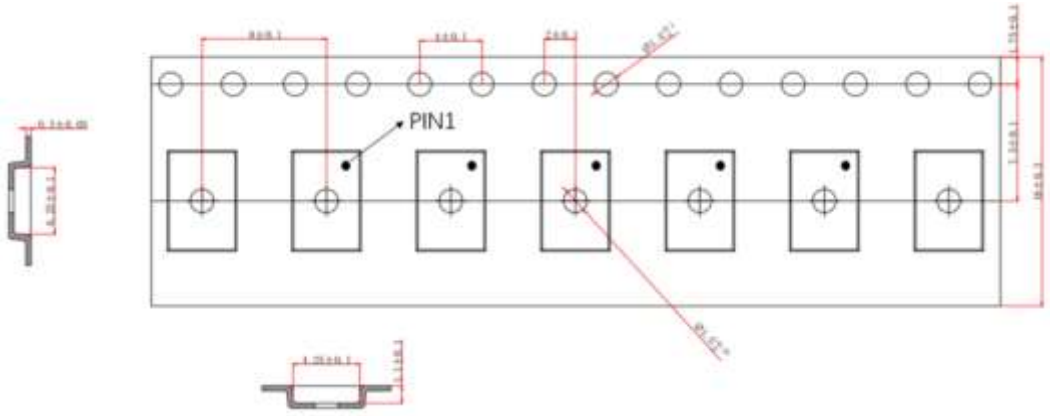


SIDE VIEW

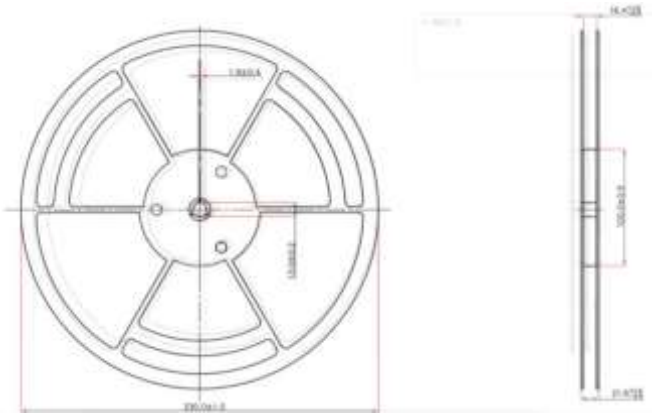
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

Reel Information



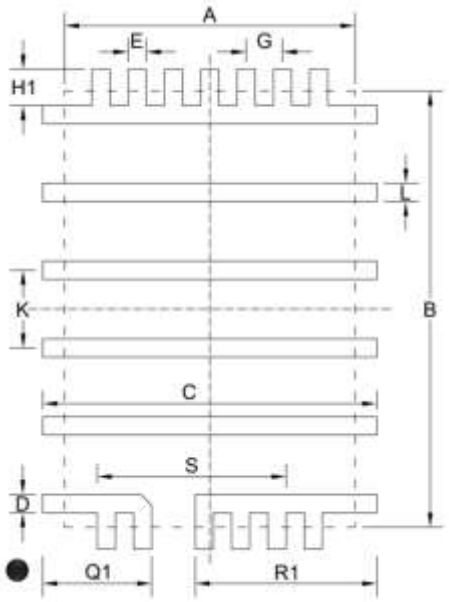
NOTES:
1, CARRIER TAPE COLOR: BLACK.
2, COVER TAPE WIDTH: 13.3±0.10.
3, COVER TAPE COLOR: TRANSPARENT.
4, 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20 MAX.
5, CAMBER NOT TO EXCEED 1MM IN 100MM.
6, MOLD# QFN/DFN/MIS6X4X0.75/0.85.
7, ALL DIMS IN MM.
8, BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.



NOTES:
1. 2500 UNITS PER TRAY.
2. COLOR: WHITE.
3. ALL DIM IN mm.
4. GENERAL TOLERANCE±0.25.
5. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.
6. THE DERECTION OF VIEW:

Land Pattern

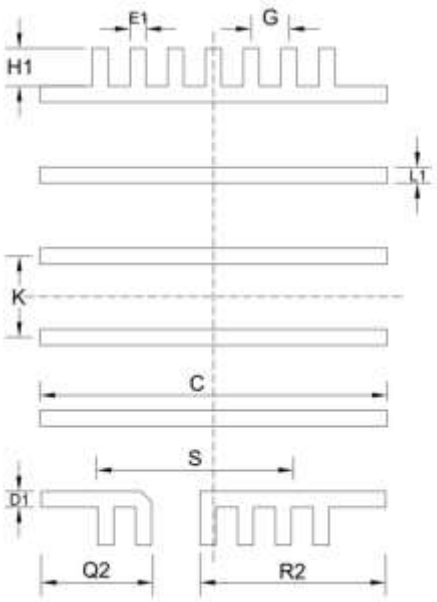
Recommended Land Pattern



Unit: mm

SYMBOL	MILLIMETER	NOTE
A	4.0	
B	6.0	
C	4.6	5X
D	0.25	3X
E	0.25	13X
G	0.5	10X
H1	0.5	13X
K	1.07	6X
L	0.25	4X
R1	2.5	
Q1	1.5	
S	2.6	

Recommended Stencil Drawing



Unit: mm

SYMBOL	MILLIMETER	NOTE
C	4.56	5X
D1	0.21	3X
E1	0.21	13X
G	0.5	10X
H1	0.5	13X
K	1.07	6X
L1	0.21	4X
R2	2.46	
Q2	1.46	
S	2.6	

Revision History

Major changes since the last Revision

Revision	Date	Description of Changes
1.0	2025-11-22	Version 1.0 Release
1.1	2025-12-15	Version 1.1 Release